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PATENT APPLICATION

JC1 Sec'd PCT/PTO 24 MAY 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: US National Stage of PCT/JP00/06824

Filed: May 24, 2001

4 / IDS
E. Willis
11-15-01

Docket No.: 109609

For: INTERCONNECT SUBSTRATE, SEMICONDUCTOR DEVICE, METHODS OF FABRICATING, INSPECTING, AND MOUNTING THE SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

INFORMATION DISCLOSURE STATEMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- 2. The references were cited in a counterpart foreign application. An English language version of the foreign search report is attached for the Examiner's information.
- 3. English-language Abstracts of JP A 4-150055 and JP A 3-245591 are attached hereto.

Respectfully submitted,


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